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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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*Ex parte* MORTEZA CYRUS AFGHAHI and ESIN TERZIOGLU

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Appeal 2008-2836
Application 10/795,825
Technology Center 2800

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Decided: September 11, 2008

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Before KENNETH W. HAIRSTON, JOHN A. JEFFERY, and ELENI MANTIS MERCADER, *Administrative Patent Judges*.

MANTIS MERCADER, *Administrative Patent Judge*.

DECISION ON APPEAL

## STATEMENT OF THE CASE

Appellants seek our review under 35 U.S.C. § 134 of the Examiner's rejection of claims 1 and 5-8. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

## INVENTION

Appellants' claimed invention is directed to a single-ended sense amplifier having a DataIn voltage sampled and stored as a reference voltage at node 1021 just before a measurement is taken, thereby making the circuit substantially independent of ground or supply voltage references (Spec. 34:5-15).

Claim 1, reproduced below, is representative of the subject matter on appeal:

1. A sense amplifier, comprising:

a sampling circuit receiving an input signal to the sense amplifier;

a reference node operable to store a reference signal corresponding to the input data, the reference signal serving as a reference voltage of the sense amplifier;

a timing circuit activating the sampling circuit a predetermined interval before measurement of the input signal is initiated, the sampling circuit admitting the input signal to the reference node thereby.

## THE REJECTION

The Examiner relies upon the following as evidence of unpatentability:

| | | |
|---|---|---|
| Pilo | US 5,343,428 | Aug. 30, 1994 |

The following rejection is before us for review:

Claims 1 and 5-8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Pilo.

## ANTICIPATION

There are two anticipation issues before us regarding whether Appellants have shown that the Examiner erred in rejecting claims 1 and 5-8 under 35 U.S.C. § 102(b).

The first issue is whether the Examiner erred in determining that Pilo teaches a reference node that serves as a reference voltage of a sense amplifier. The first issue turns on whether a "reference node" under the broadest reasonable interpretation can be construed as a node having a voltage used as a point of reference. The second issue is whether the Examiner erred in determining that Pilo teaches a timing circuit activating the sampling circuit at a predetermined interval before measurement of the input signal is initiated. The second issue turns on whether Pilo teaches "a predetermined interval" before measurement of the input signal.

## FINDINGS OF FACT

The relevant facts include the following:

1. Appellants' Specification states that transistors 1025 and 1026 add capacitance to the node 1021 (Spec. 34:13-14).
2. Appellants' claim 1 recites that the reference node stores a reference signal corresponding to the input signal (claim 1).

3. Pilo teaches nodes 101 and 102 (either one of which can be interpreted as a reference node) storing signals MUXLAT and MUXLAT* and wherein capacitor-connected transistors 57 and 56 add capacitance to the nodes 101 and 102, respectively (Pilo's Fig. 1).
4. Pilo teaches that the external clock signal CLK is converted to complimentary internal clock signals K and K* by inverters 36, 37, and 38 (col. 5, ll. 5-7).
5. Pilo teaches that "[t]ransfer gate 40 provides a relatively small interval of gate delay," thereby ensuring that as internal clock signals K and K* transition from one logic gate to another, they cross each other at substantially the midpoint of their swings (col. 5, ll. 5-11).
6. Pilo teaches that when the CLK signal is high the transfer gates 46 and 49 become conductive allowing signals MUXLAT and MUXLAT* to be provided to the differential amplifier 25 (col. 5, ll. 12-16).
7. Pilo teaches that measurement of the input signals MUXLAT and MUXLAT* is initiated at transistors 26 and 27 as shown in Figure 1.

## PRINCIPLES OF LAW

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. Inc., v. Union Oil Co. of Calif.*, 814 F.2d 628, 631 (Fed. Cir. 1987).

Analysis of whether a claim is patentable over the prior art under 35 U.S.C. § 102 begins with a determination of the scope of the claim. We determine the

scope of the claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004).

The claim terms should be given their broadest reasonable meaning in their ordinary usage as such claim terms would be understood by one skilled in the art by way of definitions and the written description. *In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997).

> The claims, of course, do not stand alone. Rather, they are part of a 'fully integrated written instrument' . . . consisting principally of a specification that concludes with the claims. For that reason, claims 'must be read in view of the specification, of which they are a part.' . . . . [T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'

*Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005).

During ex parte prosecution, claims must be interpreted as broadly as their terms reasonably allow since applicants have the power during the administrative process to amend the claims to avoid the prior art. *In re Zletz*, 893 F.2d 319, 322 (Fed. Cir. 1989).

Claim terms are presumed to have their customary and ordinary meaning unless there is an express intention to impart the novel meaning of the claim terms. *Sunrace Roots Enterprise Co., Ltd. v. SRAM Corp.*, 336 F.3d 1298, 1302 (Fed. Cir. 2003).

Although claims are interpreted in light of the specification, limitations from the specification are not read into the claims. *In re Van Geuns*, 988 F.2d 1181,

1184 (Fed. Cir. 1993).

> If the prior art reference does not expressly set forth a particular element of the claim, that reference still may anticipate if that element is 'inherent' in its disclosure. To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.' 'Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'

*In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999) (internal citations omitted).

## ANALYSIS

Initially, we note that claims 1 and 5-8 were argued as a group with claim 1 as representative (Br. 4-8).[1] Accordingly, claims 5-8, which are subject to the same ground of rejection, fall with claim 1 from which they depend. *See* 37 C.F.R. § 41.37 (c)(1)(vii) (2004).

> *a) Did the Examiner err in determining that Pilo teaches a reference node that serves as a reference voltage of a sense amplifier as claimed?*

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[1] Only arguments made by Appellants have been considered in this decision. Arguments which Appellants could have made but did not make in the Brief have not been considered and are deemed waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2004).

Appellants argue that "[t]he terms "reference node," "reference signal" and "reference voltage" are terms of art that are well understood by those skilled in the art of sensing amplifiers as referring to a reference point to which a single-ended input signal is compared" (Br. 4). Appellants further argue that Pilo's sense amplifier 20 is a differential amplifier which does not make use of a reference voltage at all (Br. 5).

The Examiner responds that the claims do not recite "a single-ended input signal" and thus, Appellants are attempting to read a limitation from the Specification into the claims (Ans. 4). Furthermore, the Examiner states that in the absence of special definition of the term "reference node," the terms are interpreted under the broadest reasonable interpretation to simply mean a node having a voltage that is used as a point of reference (i.e., a comparison voltage) (Ans. 4). The Examiner further clarifies that as shown in Appellants' Figure 10, the reference node is a capacitive node having a data signal applied thereto, which is exactly what Pilo shows in Figure 1 with node 101 (Ans. 4).

We agree with the Examiner's findings of facts and conclusions as set out in the Answer and adopt them as our own. We add the following primarily for emphasis.

Appellants' Specification states that transistors 1025 and 1026 add capacitance to the node 1021 (Finding of Fact 1). Further, Appellants' claim 1 recites that the reference node stores a reference signal corresponding to the input signal (Finding of Fact 2). Similarly, Pilo teaches nodes 101 and 102 (either one of which can be interpreted as a reference node) storing signals MUXLAT and

MUXLAT* and wherein capacitor-connected transistors 57 and 56 add capacitance to the nodes 101 and 102, respectively (Finding of Fact 3). Furthermore, in the absence of any special definition, reference nodes 101 and 102 can be reasonably interpreted to mean a node having a voltage that is used as a point of reference.

Thus, as stated *supra*, the "reference node" was accorded the broadest reasonable construction in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d at 1364. Furthermore, the limitation "a single-ended input signal" is appropriately not read into the claims. *In re Van Geuns*, 988 F.2d at 1184.

Thus, Appellants' argument has not persuaded us of error in the Examiner's rejection of claim 1 because the "reference node" was given its broadest reasonable interpretation in light of the specification and the limitation of "a single-ended input signal" was appropriately not read into the claims (Findings of Fact 1-3).

*b) Did the Examiner err in determining that Pilo teaches a timing circuit activating the sampling circuit a predetermined interval before measurement of the input signal is initiated as claimed?*

Appellants state that the measurement of the input signals in Pilo is initiated when the CLK signal activates the transmission gates 40, 43, and 52 (Br. 7). Therefore, "the CLK signal of Pilo cannot be said to activate the sampling circuit (transmission gates 40, 43, and 52) *a predetermined time before* measurement of the input signal is *initiated*" (emphasis in original) (Br. 7).

The Examiner responds that Pilo's clock signal is initially applied to the sampling circuit to activate it, and then once the sampling circuit has been activated, the input signal (i.e., MUXLAT and MUXLAT*) is able to pass through to the control terminals of transistors 26 and 27, which allows the measurement of the input signal to take place (Ans. 6).

We agree with the Examiner's findings of facts and conclusions as set out in the Answer, which address the timing circuit activating the sampling circuit *before* the measurement of the input signal is initiated (emphasis added). Furthermore, it is undisputed that Pilo's "sampling circuit" is the combination of inverters 36, 37, and 38 and transmission gates 40, 43, and 52 (Br. 6). However, we still need to address whether Pilo teaches activation of the sampling circuit occurring "a predetermined interval" before the measurement of the input signal as recited in claim 1.

Pilo teaches that the external clock signal CLK is converted to complimentary internal clock signals K and K* by inverters 36, 37, and 38 (Finding of Fact 4). Furthermore, Pilo teaches that transfer gate 40 provides a relatively small interval of gate delay, thereby ensuring that as internal clock signals K and K* transition from one logic gate to another, they cross each other at substantially the midpoint of their swings (Finding of Fact 5). Finally, Pilo teaches that when the CLK signal is high the transfer gates 46 and 49 become conductive allowing signals MUXLAT and MUXLAT* to be provided to the differential amplifier 25 (Finding of Fact 6). Thus, it necessarily follows that the activation of the sampling circuit occurs at a "predetermined interval" defined by the delays caused by component

tolerances of inverters 36, 37, 38, and transmission gates 40, 43, and 52 much like the explicitly stated interval gate delay of transfer gate 40 (Finding of Fact 5). The interval (i.e., component delays) is necessarily predetermined to allow the internal clock signals K and K* to transition from one logic gate to another and to cross each other at substantially the midpoint of their swings accounting for delays as evidenced by the explicitly gate delay of transfer gate 40 (Finding of Fact 5).

Furthermore, the activation of the sampling circuit (i.e., inverters 36, 37, 38, and transmission gates 40, 43, and 52) occurs at a predetermined interval (i.e., predetermined component delays) before measurement of the input signal is initiated (i.e., measurement of the input signals MUXLAT and MUXLAT* is initiated at transistors 26 and 27 (Finding of Fact 7) and as indicated in Ans. 6).

Thus, Appellants' argument has not persuaded us of error in the Examiner's rejection of claim 1 because Pilo teaches a timing circuit activating the sampling circuit *a predetermined interval* before measurement of the input signal is initiated (Findings of Fact 4-7) (emphasis added).

## CONCLUSION OF LAW

We conclude that Appellants have not shown that the Examiner erred in rejecting claims 1 and 5-8 under 35 U.S.C. § 102(b).

## ORDER

The decision of the Examiner to reject claims 1 and 5-8 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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